IN THE CLAIMS:

Please amend the claims as shown in the following claims listing.

1. (Currently amended) A cache memory subsystem comprising:
a cache storage configured to store a plurality of cache lines of data;
a scheduler configured to schedule reads and writes of information ~~associated with~~ to said cache storage using a fixed latency pipeline;
wherein in response to scheduling a read request to said cache storage, said scheduler is further configured to cause an associated write to said cache storage to occur a fixed number of cycles after said scheduling a read request.

2. (Currently amended) The cache memory subsystem as recited in claim 1, wherein said associated write corresponds to a cache line of victim data which has been evicted from a higher-level cache in response to a read miss of said higher-level cache.

3. (Currently amended) The cache memory subsystem as recited in claim 2, wherein said scheduler is further configured to perform said associated write to a storage location within said cache storage having an address corresponding to said cache line of victim data.

4. (Original) The cache memory subsystem as recited in claim 1, wherein said associated write corresponds to a cache line of fill data from a system memory.

5. (Original) The cache memory subsystem as recited in claim 4, wherein said scheduler is further configured to perform said associated write to a storage location within said cache storage having an address corresponding to said read request.

6. (Original) The cache memory subsystem as recited in claim 1, wherein in response to scheduling said read request, said scheduler is further configured to provide an indication that said read request is scheduled and that a read response will follow.

7. (Original) The cache memory subsystem as recited in claim 6, wherein said scheduler is further configured to provide said indication a predetermined amount of time before said read response.

8. (Original) The cache memory subsystem as recited in claim 7, wherein said predetermined amount of time is programmable.

9. (Original) The cache memory subsystem as recited in claim 1 further comprising a tag storage configured to store a plurality of tags each corresponding to a respective cache line of said plurality of cache lines.

10. (Currently amended) A method comprising:

storing a plurality of cache lines of data in a cache storage;

scheduling reads and writes of information ~~associated with~~ to said cache storage using a fixed latency pipeline;

wherein in response to scheduling a read request to said cache storage, causing an associated write to said cache storage to occur a fixed number of cycles after said scheduling a read request.

11. (Currently amended) The method as recited in claim 10, wherein said associated write corresponds to a cache line of victim data which has been evicted from a higher-level cache in response to a read miss of said higher-level cache.

12. (Original) The method as recited in claim 11 further comprising performing said associated write to a storage location within said cache storage having an address corresponding to said cache line of victim data.

13. (Original) The method as recited in claim 10, wherein said associated write corresponds to a cache line of fill data from a system memory.

14. (Original) The method as recited in claim 13 further comprising performing said associated write to a storage location within said cache storage having an address corresponding to said read request.

15. (Original) The method as recited in claim 10 further comprising providing an indication that said read request is scheduled and that a read response will follow in response to scheduling said read request.

16. (Original) The method as recited in claim 15 further comprising providing said indication a predetermined amount of time before said read response.

17. (Original) The method as recited in claim 16, wherein said predetermined amount of time is programmable.

18. (Currently amended) A microprocessor comprising:
an execution unit configured to execute instructions and operate on data;
a higher-level cache memory subsystem coupled to store a first plurality of cache lines of said data in a first cache storage;
a lower-level cache subsystem coupled to said higher-level cache subsystem,
wherein said lower-level cache subsystem includes:
a second cache storage configured to store a second plurality of cache lines of said data ~~in a second cache storage~~;
a scheduler configured to schedule reads and writes of information ~~associated with~~ to said second cache storage using a fixed latency pipeline;
wherein in response to scheduling a read request from said higher-level cache subsystem, said scheduler is further configured to cause an

associated write to said second cache storage to occur a fixed number of cycles after said scheduling a read request.

19 [18]. (Currently amended) The microprocessor as recited in claim [17] 18, wherein said associated write corresponds to a cache line of victim data which has been evicted from a higher-level cache in response to a read miss of said higher-level cache.

20 [19]. (Currently amended) The microprocessor as recited in claim [18] 19, wherein said scheduler is further configured to perform said associated write to a storage location within said cache storage having an address corresponding to said cache line of victim data.

21 [20]. (Currently amended) The microprocessor as recited in claim [17] 18, wherein said associated write corresponds to a cache line of fill data from a system memory.

22 [21]. (Currently amended) The microprocessor as recited in claim [20] 19, wherein said scheduler is further configured to perform said associated write to a storage location within said cache storage having an address corresponding to said read request.

23 [22]. (Currently amended) The microprocessor as recited in claim [17] 18, wherein in response to scheduling said read request, said scheduler is further configured to provide an indication for said higher-level cache memory subsystem that said read request is scheduled and that a read response will follow.

24 [23]. (Currently amended) The microprocessor as recited in claim [22] 23, wherein said scheduler is further configured to provide said indication a predetermined amount of time before said read response.

25 [24]. (Currently amended) The microprocessor as recited in claim [23] 24, wherein said predetermined amount of time is programmable.

26 [25]. (Currently amended) The microprocessor as recited in claim [17] 18, wherein said higher-level cache memory subsystem is a level one (L1) cache and said lower-level cache memory subsystem is a level two (L2) cache.